

# 2SK3539

## Silicon N-channel MOSFET

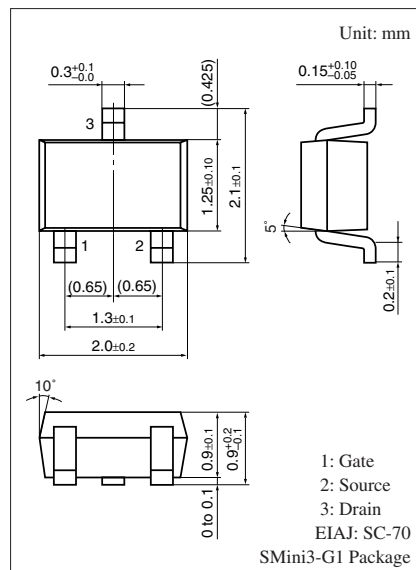
For switching

### ■ Features

- High-speed switching
- Wide frequency band
- Gate protection diode built-in

### ■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Drain-source voltage	$V_{DS}$	50	V
Gate-source voltage (Drain open)	$V_{GSO}$	$\pm 7$	V
Drain current	$I_D$	100	mA
Peak drain current	$I_{DP}$	200	mA
Power dissipation	$P_D$	150	mW
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$



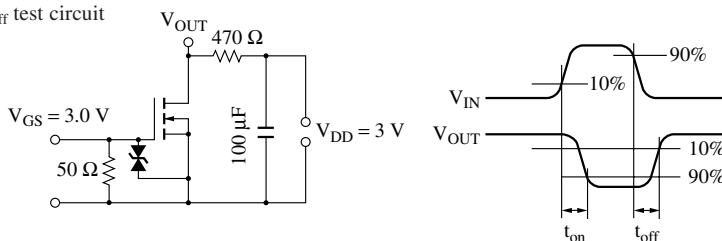
Marking Symbol: 5F

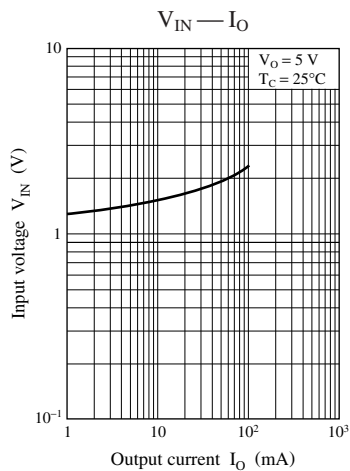
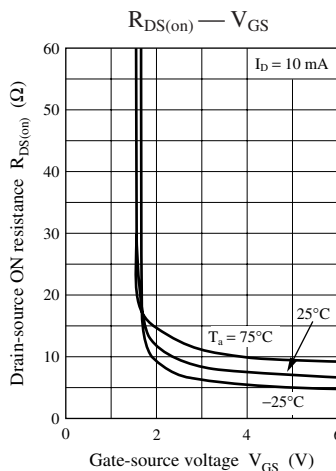
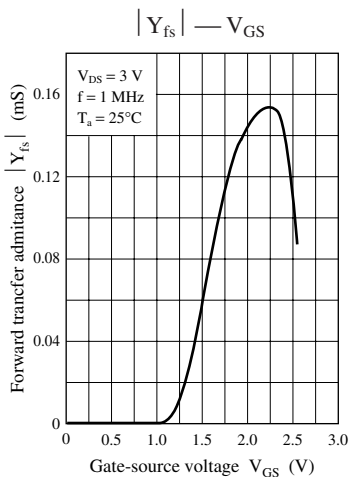
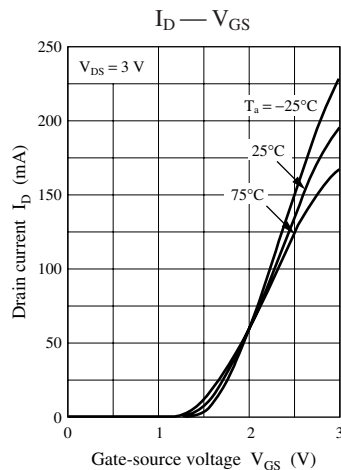
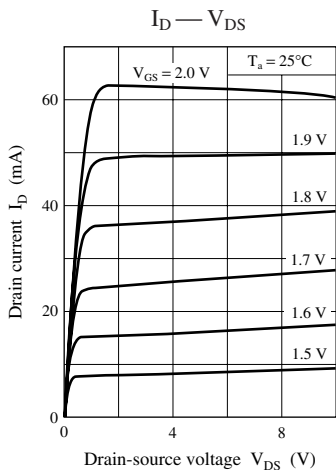
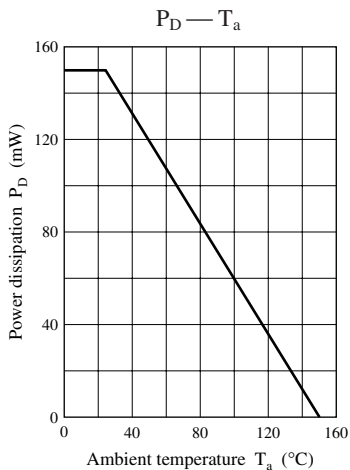
### ■ Electrical Characteristics $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source surrender voltage	$V_{DSS}$	$I_D = 10 \mu\text{A}, V_{GS} = 0$	50			V
Drain-source cutoff current	$I_{DSS}$	$V_{DS} = 50 \text{ V}, V_{GS} = 0$			1.0	$\mu\text{A}$
Gate-Source cutoff current	$I_{GSS}$	$V_{GS} = \pm 7 \text{ V}, V_{DS} = 0$			$\pm 5.0$	$\mu\text{A}$
Gate threshold voltage	$V_{th}$	$I_D = 1.0 \mu\text{A}, V_{DS} = 3 \text{ V}$	0.9	1.2	1.5	V
Drain-source ON resistance	$R_{DS(on)}$	$I_D = 10 \text{ mA}, V_{GS} = 2.5 \text{ V}$		8	15	$\Omega$
		$I_D = 10 \text{ mA}, V_{GS} = 4.0 \text{ V}$		6	12	
Forward transfer admittance	$ Y_{fs} $	$I_D = 10 \text{ mA}, V_{DS} = 3 \text{ V}, f = 1 \text{ kHz}$	20	60		mS
Short-circuit forward transfer capacitance (Common source)	$C_{iss}$	$V_{DS} = 3 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$		12		pF
Short-circuit output capacitance (Common source)	$C_{oss}$			7		pF
Reverse transfer capacitance (Common source)	$C_{rss}$			3		pF
Turn-on time *	$t_{on}$	$V_{DD} = 3 \text{ V}, V_{GS} = 0 \text{ V to } 3 \text{ V}, R_L = 470 \Omega$		200		ns
Turn-off time *	$t_{off}$	$V_{DD} = 3 \text{ V}, V_{GS} = 3 \text{ V to } 0 \text{ V}, R_L = 470 \Omega$		200		ns

Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

2. \*:  $t_{on}, t_{off}$  test circuit





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